IN THE CLAIMS

The following is a listing of the claims in the application with claims 1 and 3 shown as currently amended and with claim 5 added and with claim 2 shown as cancelled:

Listing of Claims:

1. (currently amended) A signal output circuit for controlling output of an input signal, comprising:

an internal circuit;

a digital delay circuit ~~delaying~~ configured to delay, by digital processing, a control signal for controlling an operation of the internal circuit; and

a switch ~~muting~~ configured to mute the input signal in accordance with an output of the digital delay circuit,

wherein the control signal is a shutdown signal shutting down the internal circuit.

2. (canceled).

3. (currently amended) The signal output circuit as claimed in claim [2] 1, wherein a period of time for which the control signal is delayed by the digital delay circuit is set so that the muting of the input signal is canceled after the internal circuit is activated based on the control signal.

4. (original) The signal output circuit as claimed in claim 1, wherein the digital delay circuit comprises a logic timer.

5. (New) The signal output circuit as claimed in claim 1, further comprising:

an amplifier circuit configured to amplify the input signal by comparing the input signal with a reference voltage;

a reference voltage generator circuit configured to generate the reference voltage, the reference voltage gradually increasing in response to cancellation of the shutting down of the internal circuit; and

a circuit configured to bypass a resistor of the reference voltage generator circuit in response to the cancellation of the shutting down of the internal circuit until the output of the digital delay circuit cancels the muting of the input signal, so as to accelerate the gradual increase of the reference voltage.